AMENDMENTS TO THE SPECIFICATION

Please AMEND paragraph [0099] in accordance with a following:

[0099] When the second scan pulse SP is applied to a gate line succeeding the pre-stage gate line (e.g., when a second gate-on signal GOS2 is applied to the gate line GLn, succeeding the pre-stage gate line GLn-1), the third and fourth TFTs T3 and T4 of the cell drivers ~~126~~ within pixel cells PE of the EL display panel 40, connected to the gate line GLn, are maintained in the aforementioned ON state. When the third and fourth TFTs T3 and T4 are maintained in their ON states, the current stored within the second data signal controller circuit 48B (e.g., the current corresponding to the data signal outputted by the data driver 46) may be charged to corresponding ones of the storage capacitors Cst within pixel cells PE of the EL display panel 40. Subsequently, the voltage charged in the storage capacitors Cst may be applied to the gate terminal of the first TFT T1 in the pixel cells PE and the amount of current conducted between the source and drain terminals of the first TFT T1, applied from the cell drive voltage source VDD, may thereby be controlled in accordance with the outputted data signals. As a result, the OLED may emit light in accordance with the amount of current applied from the cell drive voltage source VDD and conducted between the source and drain terminals of the first TFT T1. Accordingly, current may be applied from the data signal controller circuit 48 to the pixel cells PE within the OELD panel 40 such that a luminosity value displayed by the pixel cells PE across the OELD panel 40 varies, at most, by about 30%. In one aspect of the present invention, current may be applied from the data signal controller circuit 48 to the pixel cells PE within the OELD panel 40 such that a luminosity value displayed by the pixel cells PE across the OELD panel 40 varies by about 5%